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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,048	01/22/2004	Ralf Herz	Micronas.7867	3796

7590 10/10/2006

Gauthier & Connors LLP
225 Franklin Street, Suite 3300
Boston, MA .02110

EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,048	HERZ ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 20-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. On March 23, 2006, a first office action was mailed to the applicant's representative and on very same day applicant mailed a second preliminary amendments to the claims and specification. Realizing that the first office action and the second preliminary amendments "crossed in the mail", this new (first) office action based on newly submitted (amended) specification and claims is being issued.

Response to Amendment

2. This office action is in response to applicant's communication filed on March 27, 2006. In response to applicant's second preliminary amendments, claims 1-10 have been amended and new claims 20-29 have been added. As a result, claims 1-10 and 20-29 remain pending in this application.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Objections

4. Claim 22 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 20. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is

proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 6 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 6 and 23 recites the limitation "common access control device that switches the switching device", the specification fails to describe the "common access control device" and it is not well known in the art.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

8. Claims 21, 26, 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites the limitation "an address" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 26 recites "a memory connection that facilitates connection of the memory to the information" which is vague and indefinite language.

Claim 28 recites the limitation "a processor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 29 recites the limitation "the memory" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 3, 5-10 and 20-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurafuji et al. (US 6,584,528 B1).

As per claim 1, Kurafuji teaches a storage device for a multi-bus architecture (col. 2, lines 1-25), comprising:

at least one memory that stores information (col. 4, lines 17-25);

a memory connection having a port that is connected to the at least one memory and is selectively connected to one of a plurality of buses within the multi-bus architecture (col. 4, lines 22-29);

at least one data line that communicates with the memory connection and the one of the plurality of buses to provide information to the memory connection to control the memory (col. 4, lines 5-12);

a switching device that selectively connects the memory connection to the one of the plurality of the buses to transmit information between the one of the plurality of buses and the memory (col. 4, lines 24-34).

As per claim 3, Kurafiji teaches an address analyzer connected to the memory, that analyzes addresses on address lines that form a part of at least one of the plurality of buses for determining accesses to the at least one memory and that switches switching device to a corresponding one of the plurality of buses (col. 4, lines 52-60, col. 8, lines 52-57).

As per claim 5, Kurafuji teaches an adjustable separator device, that stores a memory addresses of the at least one memory for analysis be the address analyzer (col. 5, lines 45-54).

As per claim 6, Kurafuji teaches the analyzer with common access control device that switches the switching device and one comparator per each one of the plurality of buses to compare the address with the memory address of the at least one memory (col. 2, line 63 – col. 3, line 7 and col. 5, lines 48-54, detects matching address inherently teaches comparator to match address).

As per claim 7, Kurafuji teaches a modifier that processes different types of information (col. 4, lines 60-62, a write control signal selector, col. 7, lines 26-334, data

output control signal, i.e. distinguishing between different types of data, read, write or control data).

As per claim 8, Kurafuji teaches a logic device with block loss signal to a processor in response to deviation from an executed data transfer (col. 6, lines 44-54, at a timing when a normal access is completed, the reset signal is asserted and the mode signal is deasserted).

As per claims 9 and 10, Kurafuji teaches data and command (address) memories (col. 4, lines 8-25).

As per claims 20 and 29, Kurafuji teaches a storage device for use with a bus architecture with plurality of buses (col. 2, lines 2-5), the storage device comprising:

a memory (col. 2, line 3, a single port memory);

a switching device that selectively connects the memory with one of the plurality of buses to transmit information on the selected one of the plurality of buses to the memory (col. 2, lines 4-10, col. 4, lines 24-29);

a logic device that provides an interrupt signal on line to a processor to interrupt operation of the processor whenever an access to the memory is desired by at least one of the plurality of buses (col. 4, lines 43-46, an exception signal is output to processor); and

an analyzer that analyzes an address on the address lines that form a portion of at least one of the plurality of buses, where the analyzer controls the switching device to selectively connect one of the plurality of buses to the memory depending on the address that analyzer analyzed (col. 4, lines 52-60, col. 8, lines 52-57).

Claim 21 is rejected under same rationales as applied to claim 5 above.

As per claim 22, the limitation is also a part of claim 20, (lines 10-13 of claim 20) and hence rejected under same rationales as applied to claim 20 above.

Claim 23 is rejected under same rationales as applied to claim 6 above.

Claims 24 and 25 are rejected under same rationales as applied to claim 7 above.

Claim 27 is rejected under same rationales as applied to claims 9 and 10 above.

Claim 28 is rejected under same rationales as applied to claim 8 above.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurafuji et al. (US 6,584,528 B1) {and (Rogers US 2004/0059897 A1 and (Jain US 6,789,150 B1 incorporates as an evidentiary references)}.

As per claim 2, Kurafuji teaches all the limitations of claim 1, and further teaches sending an interrupt signal to processor (col. 4, lines 43-46, an exception signal is output to processor), but fails to teach delaying of one clock cycle. It is well known in the art that bus switching requires some clock cycles (see Rogers, paragraph [0012] and Jain, col. 1, lines 45-55). Thus, it would have been obvious to one having ordinary skill

in the art at the time of the invention to provide delaying the processor by one (or several) clock cycle to allow for delay necessary to complete bus switching during successive clock cycle bus switching.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurafuji et al. (US 6,584,528 B1) as applied to claims 1 and 3 above, and further in view of Amon et al. (US 6,138, 204).

As per claim 4, Karfuji teaches all the limitations of claims 1 and 3 above but fails to teach memory accesses of address segments smaller than a width of one of the plurality of buses. Amon teaches accesses with different word widths of buses (abstract). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize teachings of Amon to access data smaller than word width of bus in the system of Kurafuji, the advantage would be the integration of various kinds of memories and buses available (Amon, col. 2, lines 34-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

9/29/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER